REMARKS

Reconsideration of this application is respectfully requested. Claims 1-29 remain pending.

Claim Rejections - 35 U.S.C. § 102

Claims 1, 2, 5, 6, 9, 11, 13, 14, 16-19, 21, 23-25 and 27-29 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,778,419 to Hansen et al. ("Hansen"). Applicant respectfully disagrees with this reason for rejection.

Claim 1 recites, in part:

> a first address and control bus connected to the first memory controller and the first memory component; and
>
> a first data bus connected to the first memory controller and to the first memory component, wherein the first data bus uses differential signaling and has a first data bus symbol time that is shorter than a first address and control bus symbol time of the first address and control bus

Hansen discloses a memory chip 100 having a memory controller 130, synchronous DRAM array 140, and high bandwidth interface divided into a packet buffer 150, receiver section 145 and transmitter section 155 (Hansen, col. 4, lines 52-67, Figure 1). Assuming *arguendo* that, as posited in paragraph 6 of the Office Action, the memory controller 130 and synchronous DRAM array 140 correspond to the first memory controller and first memory component of claim 1, and that the row and column address outputs of the packet buffer 150 (Hansen, Figure 4) correspond to the first address and control bus of claim 1, Hansen still does not disclose or suggest that the row and column address outputs of the packet buffer 150 are connected to the memory controller 130 and therefore fails to meet the limitation "a first address and control bus connected to the first memory controller and the first memory component." Further, assuming *arguendo* that the eight-bit "DATA" input (113) to the receiver section 145 corresponds to the first data bus of claim 1 as suggested in paragraph 6 of the Office Action, Hansen does not disclose or suggest the DATA input is connected to the synchronous DRAM array 140 or to the memory controller 130, and instead indicates that the DATA input is connected to I/O circuitry within input port 110 (shown in Hansen Figure 2). The output of input

port 110 is also not connected to synchronous DRAM array 140 or to the memory controller 130, but rather to address and data buffers within the packet buffer 150 (Hansen, Figure 4) and to various circuits (115, 118, 119) within the receiver section 145. With respect to address and data actually delivered to the memory chip 100 of Hansen, applicant notes that a single clock signal 114 is described as being the timing source for receipt of all incoming packets (Hansen, col. 5, line 20 – col. 6, line 3), and similarly that, with respect to address and data transferred between the packet buffer 150 and the synchronous DRAM array 140, Hansen discloses such address and data is transferred during a given state of a ring counter (Hansen, col, 8, lines 15-29). Thus, in neither case does Hansen disclose a data bus that "has a first data bus symbol time that is shorter than the first address and control bus symbol time." In view of these clear distinctions, applicant submits that Hansen fails to meet all the limitations of claim 1 and therefore does not anticipate claim 1, nor claims 2, 5 and 6 which depend from claim 1.

Claim 9 recites, in part:

> a first address and control bus connected to the first memory controller and to the first memory component; and
> a first data bus connected to the first memory controller and to the first memory component, wherein the first memory component includes a first termination structure connected to the first data bus and wherein the first data bus has a first data bus symbol time that is shorter than a first address and control symbol time of the first address and control bus

Applicant submits that, at least for the reasons given with respect to claim 1, Hansen does not disclose the above-recited limitations of claim 9 and therefore does not anticipate claim 9, nor claims 11 and 13 which depend from claim 9.

Claim 14 recites, in part:

> a first address and control bus connected to the first memory controller and to the first memory component; and
> a first data bus connected to the first memory controller and to the first memory component, wherein the first memory component includes a first termination structure connected to the

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first data bus, wherein the first data bus uses differential signaling, and wherein the first address and control bus uses non-differential signaling

Applicant submits that, at least for the reasons given with respect to claim 1, Hansen does not disclose "a first address and control bus connected to the first memory controller and to the first memory component," nor "a first data bus connected to the first memory controller and to the first memory component." Further, even if one were to assume *arguendo* that the data path actually connected to the synchronous DRAM array 140 (i.e., the data path coupled between the packet buffer 150 and the synchronous DRAM array 140 as shown in Figures 1 and 4 of Hansen) corresponds to the first data bus of claim 14, Hansen does not disclose or suggest that the data path uses differential signaling. Because Hansen fails to meet all the limitations of claim 14, Hansen does not anticipate claim 14, nor claims 16 and 17 which depend from claim 14.

Claim 18 recites, in part:

a first address and control bus connected to the first memory controller and to the first memory component; and

a first data bus connected to the first memory controller and to the first memory component, wherein the first data bus uses differential signaling and wherein the first memory component accesses a first word stored in the first memory component, the first word being wider than a first data bus width of the first data bus

Applicant submits that, at least for the reasons given with respect to claim 1, Hansen does not disclose "a first address and control bus connected to the first memory controller and to the first memory component," nor "a first data bus connected to the first memory controller and to the first memory component." Further, even if one were to assume *arguendo* that the data path actually connected to the synchronous DRAM array 140 (i.e., the data path coupled between the packet buffer 150 and the synchronous DRAM array 140 as shown in Figures 1 and 4 of Hansen) corresponds to the first data bus of claim 18, Hansen does not disclose or suggest that the synchronous DRAM array 140 accesses a word stored in the synchronous DRAM array 140 that is wider than that data path. In view of these clear distinctions, applicant submits that Hansen does not anticipate claim 18, nor claim 19 which depends from and further limits claim 18.

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Claim 21 recites, in part:

> a first address and control bus connected to the first memory controller and to the first memory component; and
>
> a first data bus connected to the first memory controller and to the first memory component, wherein the first memory controller includes a first receive circuit having a first read timing adjustment subcircuit for adjusting a first adjustable read data sampling time point for first read data sampled from the first data bus and wherein the first data bus uses differential signaling

Applicant submits that, at least for the reasons given with respect to claim 1, Hansen does not disclose "a first address and control bus connected to the first memory controller and to the first memory component," nor "a first data bus connected to the first memory controller and to the first memory component." Further, even if one were to assume *arguendo* that the data path actually connected to the synchronous DRAM array 140 (i.e., the data path coupled between the packet buffer 150 and the synchronous DRAM array 140) corresponds to the first data bus of claim 21, Hansen does not disclose or suggest that the memory controller 130 includes a receive circuit having a read timing adjustment subcircuit for adjusting a first adjustable read data sampling time point for read data sampled from that data path, nor that the data path uses differential signaling. Accordingly, Hansen does not meet all the limitations of claim 21 and therefore does not anticipate claim 21, nor claims 23 and 24 which depend from claim 21.

Claim 25 recites, in part:

> a first address and control bus connected to the first memory controller and to the first memory component; and
>
> a first data bus connected to the first memory controller and to the first memory component, wherein the first memory controller component includes a first receive circuit having a first read timing adjustment subcircuit for adjusting a first adjustable read data sampling time point for first read data sampled from the first data bus and wherein the first memory component includes a first termination structure connected to the first data bus

Applicant submits that, at least for the reasons given with respect to claim 21, Hansen does not disclose the above-recited limitations of claim 25 and therefore does not anticipate claim 25, nor claims 27-29 which depend from claim 25.

Allowable Subject Matter

Claims 3, 4, 7, 8, 10, 12, 15, 20, 22 and 26 have been objected to as being dependent upon a rejected base claim, but indicated to be allowable if rewritten in independent form to include all the limitations of the base claim and any intervening claims. Applicant acknowledges the allowability of claims 3, 4, 7, 8, 10, 12, 15, 20, 22 and 26 if so amended, but respectfully declines to amend such claims at this time in view of the foregoing remarks.

In Conclusion

Applicant respectfully submits that all pending claims are in condition for allowance. If a telephone interview would be helpful in any way, the examiner is invited to call the undersigned attorney.

A petition for a three (3) month extension of time is enclosed herewith.

Authorization is hereby given to charge deposit account 501914 for any fee deficiency associated with this Amendment.

Respectfully submitted,
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